REMARKS

This is intended as a full and complete response to the Office Action dated July 19, 2004 having a shortened statutory period for response set to expire on October 19, 2004. Claims 1-6, 12-17, 19-24 and 29-38 are pending in the application. Please reconsider the claims pending in the application for reasons discussed below.

Rejections: 35 U.S.C. § 102

Claims 1-6, 12-14, 19-24, and 34 stand rejected under 35 U.S.C. 102(b) as being anticipated by IBM Technical Disclosure Bulletin, November 1993, US (hereinafter "*IBM*").

Regarding claims 1, 12, and 19, the Examiner takes the position that IBM teaches the claimed elements of managing cache in a shared memory multiple processor computer system. Applicants respectfully submit, however, that IBM fails to teach a processor that executes a cache purge instruction that configures the processor to *purge* a cache line from the processor and *send* the cache line to at least one of a plurality of processors in the shared memory multiple processor system to update the at least one of the plurality of processors, as claimed.

In contrast, Applicants submit that *IBM* teaches a purge command sent (by a coherency unit in response to receiving a request from a source processor for exclusive access to an address) to nodes of processors that have cached copies of data. These purge commands cause all processors except the source processor to purge their cached copies, but not to send their cached copies to at least one of the plurality of (other) processors, as claimed. The source processor, on the other hand, is configured not to purge its cached copy, but rather to keep it. See p. 2 of *IBM* and the example illustrated in FIGs. 1-2.

Accordingly, Applicants submit claims 1, 12, and 19, as well as their dependents, are patentable over *IBM* and respectfully request withdrawal of this rejection. While claim 34 is listed as being rejected under *§102* it is not discussed in detail as such. Applicants presume this listing was inadvertent, noting that claim 34 is rejected under *§103*, as discussed in greater detail below.

Claims 29 and 35 also stand rejected under 35 U.S.C. 102(b) as being anticipated by *IBM*. Claims 29 and 35 originally depended from claims 1 and 19,

respectively, and were rewritten in independent format. Therefore, these claims have all the limitations of original claims from which they originally depended. Accordingly, Applicants submit these claims are also patentable over *IBM* for reasons discussed above and request removal of this rejection.

Rejections: 35 U.S.C. § 103 (IBM and AAPA)

Claim 30 stands rejected under 35 U.S.C. 103(a) as being unpatentable over *IBM*, and further in view of *AAPA (assumed to stand for "applicants' admitted prior art")*. The Examiner takes the position that *IBM* teaches the claimed elements but for marking a state of updated cache lines as *temporarily invalid*, which the Examiner states is taught by *AAPA*.

For reasons discussed above, Applicants submit that *IBM* fails to teach the claimed elements for managing cache (e.g., a processor configured to purge a cache line and send the cache line it to another processor). Further, Applicants submit that marking a state of cache lines as *temporarily invalid* is not admitted prior art. While Applicants state that a cache directory 200 may be configured as is known in the art (paragraph 30, lines 1-2), there is no statement that marking an entry as *temporarily invalid* is known in the art.

Accordingly, Applicants submit claim 30 is patentable over *IBM* and *AAPA*, and respectfully request removal of this rejection.

Rejections: 35 U.S.C. § 103 (IBM and Yates)

Claims 15-16, and 34 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *IBM*, and further in view of *Yates* (assumed to be U.S. Pat. No. 6,549,959 cited in a previous office action). The Examiner takes the position that *IBM* teaches the claimed elements, but for the purge instruction referencing at least five fields, which the Examiner states is taught by *Yates*.

For reasons discussed above, Applicants submit that IBM fails to teach the claimed elements for managing cache (e.g., a processor configured to purge a cache line and send the cache line it to another processor). Accordingly, Applicants submit these claims are patentable over *IBM* and *Yates*, and respectfully request removal of this rejection.

Rejections: 35 U.S.C. § 103 (IBM and Liu)

Claims 31-33 and 36-38 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *IBM*, and further in view of *Liu* (assumed to be U.S. Pat. No. 5,210,848 cited in a previous office action). The Examiner takes the position that *IBM* teaches the claimed elements, but for updating only one cache at a designated processor and marking a state of the updated cache line as exclusive at the designated processor, which the Examiner states is taught by *Liu*.

For reasons discussed above, Applicants submit that IBM fails to teach the claimed elements for managing cache (e.g., a processor configured to purge a cache line and send the cache line it to another processor). Accordingly, Applicants submit these claims are patentable over *IBM* and *Liu*, and respectfully request removal of this rejection.

CONCLUSION

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

Randol W. Read
Registration No. 43,876
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)